REMARKS

Claims 1-20 are pending in this application. Claims 1, 2, and 4-16 were rejected by Examiner as follows: Claims 1, 2, and 5-16 were rejected under 35 U.S.C.§102(e) as being anticipated by Matsumiya et al. (US 6,344,990); Claim 4 was rejected under 35 U.S.C.§103 as being unpatentable over Matsumiya et al. Claim 14 has been amended to overcome Examiner's rejection. Figure 5 of the Drawings was objected to for minor informalities and has been amended to correct said informalities. Applicants note with appreciation the Examiner's indication of allowable subject matter in Claim 3.

Independent Claim 1 of the present invention reads: "A memory array system comprising a plurality of memory cells arranged in a data array and wordline decoding circuitry for receiving a control signal for activating one of a single wordline and at least two wordlines of a plurality of wordlines traversing the plurality of memory cells during a data array accessing cycle." In contrast to Claim 1, Matsumiya discloses no single embodiment capable of both single wordline and dual wordline activation. Matsumiya discloses instead distinct embodiments, one embodiment capable of receiving a control signal for activating a single wordline, the other embodiment capable of receiving a control signal for activating two wordlines (see Matsumiya column 12, lines 55-67, specifically distinguishing the twin-cell DRAM of Matsumiya Fig. 8 from the twin-cell DRAM of Matsumiya Fig. 1). Further, Matsumiya teaches away from the invention of Claim 1. Matsumiya teaches specifically the advantages of twin-cell DRAM operation, and makes no mention of a system capable of operating both as single-cell and twin-cell DRAM, or of any other reason to create an embodiment capable of both single and dual wordline

activation (see, e.g., Matsumiya column 2, lines 54-59). Therefore, Claim 1 of the present invention is not anticipated by Matsumiya.

Claims 2-9 depend from Claim 1, therefore Claims 2-9 are not anticipated by Matsumiya for at least the reasons that Claim 1 is not anticipated by Matsumiya.

Independent Claim 10 claims, in relevant part: "...means for activating one of a single wordline and at least two wordlines of a plurality of wordlines traversing the plurality of memory cells during a data array accessing cycle." This element of Claim 10 is similar to the element used above to distinguish Claim 1 from Matsumiya. Therefore, Claim 10 is not anticipated by Matsumiya for at least the reasons that Claim 1 is not anticipated by Matsumiya.

Claims 11-13 depend from Claim 10, therefore Claims 11-13 are not anticipated by Matsumiya for at least the reasons that Claim 10 is not anticipated by Matsumiya.

As amended, independent Claim 14 reads, in relevant part: "...wordline activation circuitry for enabling single wordline activation or dual wordline activation according to said received at least one control signal." In contrast to Claim 14, Matsumiya discloses no single embodiment capable of both single wordline and dual wordline activation. Matsumiya discloses instead distinct embodiments, one embodiment capable of receiving a control signal for activating a single wordline, the other embodiment capable of receiving a control signal for activating two wordlines (see Matsumiya column 12, lines 55-67, specifically distinguishing the twin-cell DRAM of Matsumiya Fig. 8 from the twin-cell DRAM of Matsumiya Fig. 1). Further, Matsumiya teaches away from the invention of Claim 14. Matsumiya teaches specifically the advantages of twin-cell DRAM operation,

and makes no mention of a system capable of operating both as single-cell and twin-cell DRAM, or of any other reason to create an embodiment capable of both single and dual wordline activation (see, e.g., Matsumiya column 2, lines 54-59). **In addition, unlike Claim 14, Matsumiya makes no reference to using a control signal to switch between single wordline activation and dual wordline activation.** Therefore, Claim 14 of the present invention is not anticipated by Matsumiya.

Claims 15 and 16 depend from Claim 14, therefore Claims 15 and 16 are not anticipated by Matsumiya for at least the reasons that Claim 14 is not anticipated by Matsumiya.

Claim 4 reads, in relevant part: "The memory array system according to claim 2, wherein said wordline activating means includes a first and a second line shifter and a wordline driver circuit having wordline drivers for activating a respective one of the plurality of wordlines." Matsumiya teaches away from use of a second line shifter in wordline activation, instead teaching use of ground voltage (see Matsumiya column 10, lines 23-30). Therefore, Claim 4 is not made obvious by Matsumiya.

Claims 17-20 have been canceled without prejudice.

Applicants submit that pending Claims 1-16 are believed to be in condition for allowance. Allowance is respectfully requested. Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicants' attorney at the number given below.

Respectfully submitted,

Paul J. Farrell
Reg. No. 33,494
Attorney for Applicants

DILWORTH & BARRESE, LLP
333 Earle Ovington Blvd.
Uniondale, New York 11553
Tel: (516) 228-8484